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Optimized Asymmetric Multilevel Inverter with Smart Control for Efficient Renewable Grid Systems

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Abstract: In our study, we present a new Smart Control-Driven Asymmetric Multilevel Inverter (SCDAMLI) which is aimed to minimize the quantity of power semiconductor switches and maximize the quantity of levels of the output voltages. The inverter overcomes major issues of efficient and quality power conversion especially in systems of renewable energy as well as in the application of electric vehicles (EV). The suggested cross-structured architecture greatly reduces the number of components by optimizing switch set-up to make the system small and less expensive. A boost converter coupled with an improved ANFIS-based Maximum Power Point Tracking (MPPT) algorithm is utilized in order to make a solar photovoltaic (PV) module as efficient as possible in terms of energy recovery. Although multilevel inverters have advantages of a better power quality, it is known to have reliability issues due to total harmonic distortion (THD) and complicated circuitry. The SCDAMLI eliminates these shortcomings by providing 23 output voltage levels with asymmetric DC sources, providing better performance with fewer components. The inverter switching is controlled by an intelligent Teaching Learning Based Optimization (TLBO) algorithm, which guarantees good quality of voltage output and has a much lower THD. Under varying operating conditions, the system performance is assessed using the MATLAB/SIMULINK. It has been found that with the addition of an appropriately designed LC output filter, the inverter output meets IEEE standard 519 harmonic requirements, and hence is suitable in grid-connected renewable energy and electric vehicle systems.

Keywords: Asymmetric Multilevel Inverter, Reduced Switch Topology, Teaching–Learning-Based Optimization (TLBO), ANFIS-Based MPPT, Smart Control Strategies, Renewable Energy Integration.

1. Introduction

The ability to produce high-quality output voltages with smaller total harmonic distortion (THD) and with less voltage stress across power switches has made multilevel inverters (MLIs) a staple in the medium and high-power applications [1]. The latter characteristics make MLIs especially appealing to renewable energy connections, electric vehicle (EV) motors, and Flexible AC Transmission Systems (FACTS).

The CHB inverter has become popular because of its modular form and simplicity of design, and does not require sophisticated clamping or balancing circuits, among the other MLI topologies, including flying capacitor (FC), diode-clamped (neutral-point clamped, NPC) and cascaded H-bridge (CHB) [2]. Nevertheless, traditional CHB inverters need many semiconductor switches and isolated DC sources that enhance the cost of the system, control complexity, and overall reliability [3].

In a bid to overcome such constraints, various modified topologies have been suggested such as E-type, T-type and hybrid CHB [4]. Although such designs are attempting to minimize the number of components or enhance efficiency, they tend to still be based on a large number of switches or auxiliary elements. Incidentally, diode-clamped MLIs and flying capacitor MLIs need several clamping diodes, balancing capacitors, or DC-link capacitors, making it more complex to package and control the system, especially in high-voltage systems [5]. Moreover, balancing of capacitor voltages is a tasking issue, which does not only influence long term stability, but also performance

Recently, hybrid asymmetric MLIs (HAMLI) have become a promising way to solve the problem of attaining high number of voltage levels using less power electronic components [6]. Asymmetric MLIs are able to provide a greater range of output voltages than

symmetric ones because of this capability through the use of unequal DC source values [7]. A number of hybrid topologies have been suggested that take advantage of this concept. As an example, hybrid structures with transformers have high voltage but are larger and more expensive. Other topologies incorporate characteristics of packed U-cell (PUC) inverter and CHBMLI, or use diode-bypassed transistors to enhance fault tolerance.

Although these solutions are promising, most of them are associated with trade-offs like high peak inverse voltage (PIV), use of transformer, or non-easy-to-understand control schemes. Further optimization of MLI designs through simplified, lower-cost, and efficient designs with fewer switches is still an important area of study.

In order to address the difficulties of conventional and hybrid MLI topologies, the paper will suggest a new intelligent asymmetric multilevel inverter (AMLI) with optimized reduced-switch architecture [8]. Design ensures that the semiconductor switches are considerably minimized and the use of unequal DC voltage sources helps to create 23 different levels of output voltages, which not only enhances the quality and efficiency of power, but also, reduces the semiconductor switches [9].

The algorithm used to optimize energy collection of solar photovoltaic (PV)-based modules is a boost converter in combination with a Maximum Power Point Tracking (MPPT) algorithm based on Adaptive Neuro-Fuzzy Inference System (ANFIS).In addition, switching strategy is controlled by a Teaching-Learning based optimization (TLBO) algorithm that is applied through Sinuoidal Pulse Width Modulation (SPWM) with Phase Disposition (PD) carrier approach [10]. This smart control scheme guarantees a high quality of the voltage output at low THDs and less switching stresses.

The suggested architecture will utilize only two switches to be at the basic frequency with the rest of the switches being at higher frequencies thus minimizing conduction and switching losses [11]. Also the inverter has a smaller PIV than traditional topologies, which further increases reliability.

The key contributions and the novelties of this study can be summarized as follows:

a ***Fewer Switch Count:*** The proposed inverter topology uses much fewer power semiconductor switches than the traditional multilevel inverters (MLIs). Such a reduction will result in smaller sizes of the systems, reduced total cost and better power density.

b ***Better Power Quality:*** The inverter design produces a near-sinusoidal voltage waveform that satisfies IEEE 519 harmonic distortion limits, enabling efficient grid integration.

c ***Increased Efficiency:*** Since a reduced number of switching components are used, both conduction and switching losses are minimized. This results in increased system efficiency as well and thus the topology is very appropriate in cases of renewable energy sources that need high energy conversion efficiency.

d ***Reduced Switches:*** The minimized switches ease the circuitry and controlling approach of the gate driver, which contributed to the increased reliability of the system and its implementation. This also allows real-time control and hardware realization scalability through this simplification.

e ***Flexible and Modular Structure:*** The proposed topology has a high level of modularity and flexibility and can therefore be easily customized to a variety of renewable energy systems. Its scalable design makes it suitable in applications that involve the need of the higher voltages or the integration of multiple sources.

The Teaching Learning Based Optimization (TLBO) algorithm is used to identify the optimum switching angles that allow the least amount of harmonic distortion to be introduced to the inverter output voltage. In this work, the optimization is done off line in MATLAB. The switching angles are then applied in the PWM control strategy in the simulation. This method does not have any real-time computational cost and makes certain that the inverter works with optimum harmonic performance [12].

The paper will be structured in the following way, Section 2 outlines the workings and the design of the proposed asymmetric multilevel inverter (AMLI) topology. Section 3 exemplifies the different operational modes and voltage management techniques of the presented SCDAMLI, and the flexibility and efficiency of the presented SCDAMLI in multilevel conversion of power. Section 4 and 5 involves a comparative study in which the performance of the proposed topology is presented against some important parameter namely the number of switches, the level of voltages, and the quality of power. The simulated results and their validation are discussed in section 6. Lastly, Section 7 gives the concluding remarks and gives the future research possible directions.

2. Materials and Methods

2.1 Proposed SCDAMLI Topology

Figure 1 presents the classification of power inverters. The suggested system incorporates a solar-fed Single-Carrier Driven Asymmetric Multilevel Inverter (SCDAMLI) as an effective means of connecting renewable power to the electrical grid, Figure 2.

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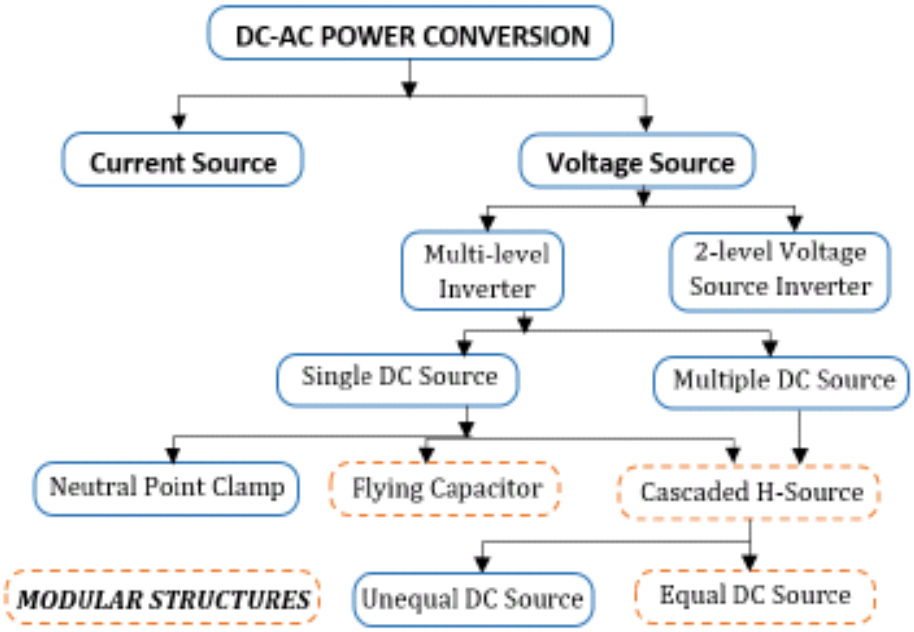


Figure 1. Ranked Classification of Power Inverter Arrangements

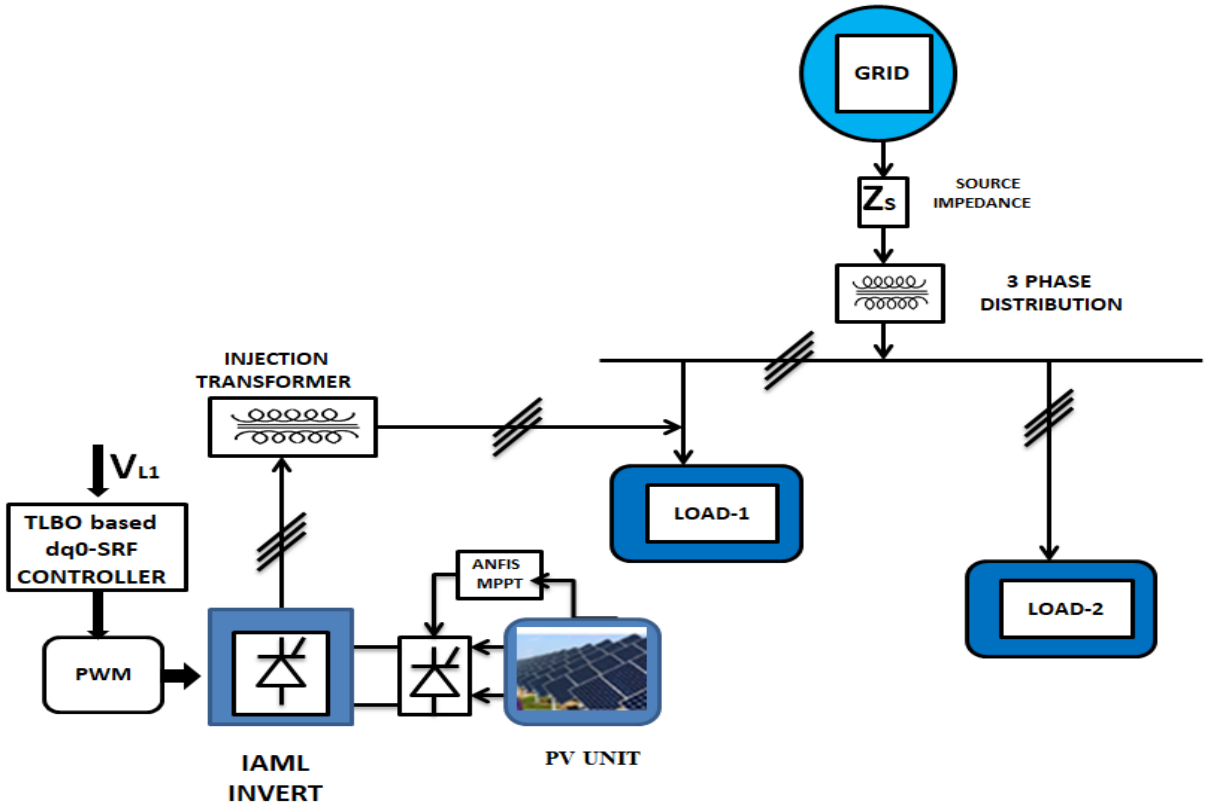


Figure 2. Suggested single-line scheme of the solar-fed SCDAMLI-based system.

The SCDAMLI combined with a Single Input Multiple Output (SIMO) boost converter is used in this arrangement to do a DC to AC conversion necessary to connect to the grid [2]. The combined structure boosts the ability to improve voltage boosting and fine output waveforms control, to increase the quality of power and system efficiency [13].

The inverter topology proposed is having three autonomous DC voltage sources (Va, Vb and Vc), seven unidirectional switches, and five bidirectional switches [14].

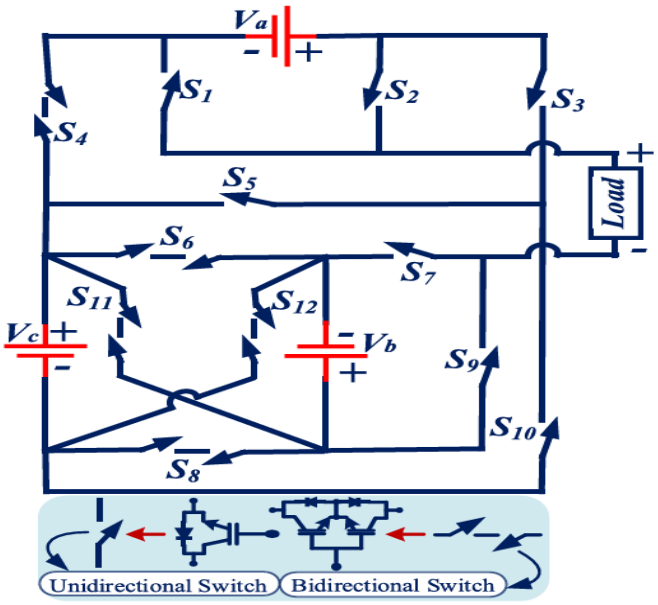


Figure 3. Setting of the proposed Single-Carrier Driven Asymmetric Multilevel Inverter (SCDAMLI)

Figure 3 shows a lattice connection of four of the bidirectional switches, making it possible to produce the voltage levels in various levels by selecting suitable switching patterns [15].

To achieve more output with fewer components, the choice of the DC voltage sources is biased towards higher output with lower components in case of asymmetric operation. The DC sources are assigned with the values as under:

$$V_a = 1V_{dc};\ V_b = 3V_{dc};\ V_c = 7V_{dc} \quad (1)$$

The topology proposed uses three isolated DC sources with an unequal ratio, to maximize the amount of attainable voltage levels and minimize the amount of switches [13]. The magnitudes of the DC sources in this work are V_a: V_b: V_c = 1:3:7. To simulate and analyze, the base voltage will be chosen as V_{dc}=50V. In this regard, the individual source values reach V_a=50V, V_b=150V and V_c=350V. Such values are continuously applied during the simulation, switching analysis, and voltage stress analysis in the manuscript. The asymmetric distribution facilitates the proposed inverter to generate a large variety of voltage levels with a small number of sources and switching devices.

Asymmetric distribution of the DC source enables the inverter to produce more levels of voltages with less switches and isolated sources thus enhancing compactness and cost-effectiveness [13].

The relationship between the number of DC sources n_{dc}^{Asy} and the number of achievable output voltage levels n_l for the asymmetric configuration is given by:

$$n_{dc}^{Asy} = \frac{(n_l-5)}{6} \quad (2)$$

On the same note, the number of switching devices n_s^{Asy} required is given as:

$$n_s^{Asy} = \frac{(n_l+1)}{2} \quad (3)$$

Because a unidirectional switch requires a specific circuit, with its own gate driver, the total gate drivers n_{gk}^{Asy} are equal to the number of switches and this is written as:

$$n_{gk}^{Asy} = n_s^{Asy} = \frac{(n_l+1)}{2} \quad (4)$$

The maximum output voltage magnitude $V_{l,\max}^{Asy}$ obtainable from the proposed configuration is given by:

$$V_{l,\max}^{Asy} = \frac{(n_l-1)}{2} \quad (5)$$

With the above set of relationships, the suggested SCDAMLI topology can generate a topology of 23 output voltage waveform levels. The voltage levels that are synthesized vary between -11V_{dc} and +11V_{dc} (including the zero point) and the expression can be stated as:

$$V_0 \in \{0, \pm V_{dc}, \pm 2V_{dc}, \ldots., \pm 11V_{dc}\} \quad (6)$$

The attainable level of output voltage is achieved by a combination of the three asymmetric sources in a proper manner. The combination of various combinations of these voltages makes possible the synthesis of several discrete levels, as the sources are chosen in the proportion of 1: 3: 7. The output voltage of the inverter may be given as

$$V0 = \pm(aV_a + bV_b + cV_c) \quad (7)$$

In which a, b, c are the switching conditions which define whether or not the respective sources are connected into the conduction path. Using V_a=1V_{dc}, V_b=3V_{dc}, and V_c=7V_{dc}, the combinations thus possible

give a range of voltage values of -11Vdc to +11Vdc. The overall number of output levels is inclusive of the zero state, which is

$N_L = 2 \times 11 + 1 = 23$ (8)

This proves the fact that the topology proposed can produce a complete voltage waveform of 23 levels without any missing intermediate states.

For asymmetric configuration,

$$n_{dc}^{Asy} = \frac{n_l - 5}{6} \quad (9)$$

Substituting $n_l = 23$:

$$n_{dc}^{Asy} = \frac{23-5}{6}$$
$$n_{dc}^{Asy} = 3 \quad (10)$$

This validates that three asymmetric DC sources are sufficient to generate 23 levels.

Table 1 gives detailed switching states of every output voltage level, both positive and negative polarities. This 23-level design has better harmonic suppression and better quality of the waveform than traditional symmetric multilevel inverter topologies.

All of the switching states in Table 1 demonstrate conduction paths unique to the inverter switches and DC sources. Once a particular combination of switches is engaged, the respective DC sources are connected to the current flow and their voltages are added to give the necessary amount of output [17]. As an example, in the $+11V_{dc}$ state, all three sources V_a, V_b and V_c contribute to the conduction path and therefore maximum positive output voltage is obtained. On the same note, intermediate levels are acquired by adding only desirable sources.

Table 1. Determining the switching state to cause 23-level output voltage in the proposed SCDAMLI

Output Voltage (Vdc)	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
+11	0	1	0	1	0	0	1	1	0	0	0	0
+10	1	0	0	1	0	0	1	1	0	0	0	0
+9	1	0	1	0	1	1	1	1	0	0	0	0
+8	0	1	0	1	0	0	0	1	1	0	0	0
+7	1	0	1	0	0	0	0	1	1	0	0	0
+6	1	0	1	0	0	0	1	1	0	1	0	0
+5	0	1	0	1	0	1	0	0	1	0	0	0
+4	0	1	0	1	0	0	1	1	0	0	0	0
+3	1	0	1	0	1	1	0	0	1	0	0	0
+2	1	0	0	1	0	0	0	1	1	0	0	0
+1	0	1	0	1	0	1	1	0	0	0	0	0
0	1	0	1	0	1	1	0	0	0	0	0	0
-1	1	0	0	1	0	0	0	1	1	0	0	0
-2	0	1	0	1	0	0	0	1	1	0	0	0
-3	0	1	1	0	0	1	0	0	1	0	0	0
-4	1	0	1	0	0	1	1	0	1	0	0	0
-5	1	0	1	0	0	1	0	0	1	1	0	0
-6	1	0	1	0	0	1	0	1	1	0	0	0
-7	0	1	1	0	0	1	0	0	1	0	0	0
-8	1	0	1	0	0	1	0	0	1	0	0	0
-9	1	0	1	0	1	0	1	1	0	0	0	0
-10	0	1	1	0	1	0	0	1	1	0	0	0
-11	1	0	1	0	1	0	0	1	1	0	0	0

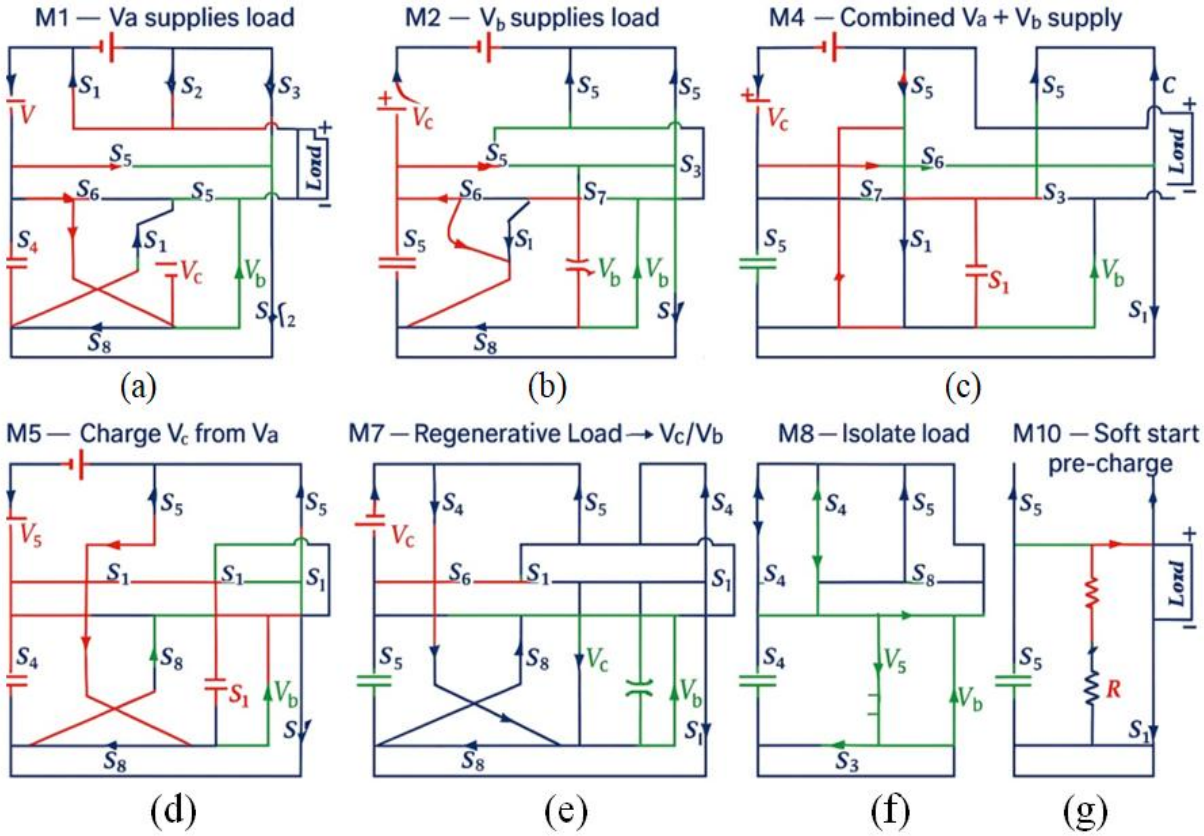


Figure 4. Principles of working of the design of a Single-Carrier Driven Asymmetric Multilevel Inverter (SCDAMLI)

The negative voltage values are obtained by reverse switching the current through the bidirectional switching network. The actual current traces of the chosen positive, zero and negative voltage values are shown in Fig. 4(a) to (g) and they confirm the accuracy of the switching states Table 1. The detailed switching states corresponding to each output voltage level, covering both positive and negative polarities, are presented in Table 1. This 23-level configuration demonstrates superior harmonic suppression and enhanced waveform quality compared to conventional symmetric multilevel inverter topologies.

$$BVM_{S1} = BVM_{S2} = BVM_{S3} = V_a = 1V_{dc}$$
$$BVM_{S7} = BVM_{S9} = V_b = 3V_{dc} \quad (11)$$
$$BVM_{S5} = BVM_{S10} = V_c = 7V_{dc}$$

$$BVM_{S4} = \frac{1}{2}(V_c + V_a) = 4V_{dc}.$$
$$BVM_{S6} = BVM_{S11} = BVM_{S8} = BVM_{S12} \quad (12)$$
$$= \frac{1}{2}(V_c + V_b) = 5V_{dc}.$$

The sum of maximum blocking voltages of the individual switches is called the total switching voltage (TSV).

$$TSV = \sum_{i=1}^{n} BVM_{Si} \quad (13)$$

The unit TSV can be represented as:

$$TSV_{PU} = \frac{TSV}{V_{L,max}} \quad (14)$$

In the proposed SCDAMLI topology, the TSV will be obtained as:

$$\begin{aligned} \mathrm{TSV^{Prop}} &= 4[5\mathrm{V_{dc}}] + 2[3\mathrm{V_{dc}}] + 2[7\mathrm{V_{dc}}] \\ &\quad + 3[\mathrm{V_{dc}}] + 4\mathrm{V_{dc}} \quad (15) \\ \mathrm{TSV^{Prop}} &= 47\mathrm{V_{dc}} \end{aligned}$$

The unit TSV of the proposed system is, therefore:

$$\mathrm{TSV_{PU}^{Prop}} = \frac{47\mathrm{V_{dc}}}{11\mathrm{V_{dc}}} = 4.27 \quad (16)$$

Table 1 shows the switching conditions in relation to the 23 levels of the output voltage of the proposed inverter. These findings indicate the voltage stress distribution and operational flexibility of the SCDAMLI, which indicate its appropriateness in multi-level conversion of power with controlled switch stress as indicated in table 2.

The conduction loss of each switch is calculated as:

$$P_{cond} = V_{on} I_{avg} + R_{on} I_{rms}^2 \quad (17)$$

Where V_{on} is the device on-state voltage drop and R_{on} is the equivalent resistance.

The switching loss is estimated as:

$$P_{sw} = f_s(E_{on} + E_{off}) \quad (18)$$

or equivalently,

$$P_{sw} = \frac{1}{2} V_{\mathrm{block}}\, I(t_{on} + t_{off}) f_s \quad (19)$$

The total inverter loss is:

$$P_{\text{loss}} = P_{\text{cond}} + P_{\text{sw}} \quad (20)$$

and the efficiency is computed as:

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} \times 100\% \quad (21)$$

These expressions have been added to the updated manuscript to provide a quantitative measure of the enhanced efficiency argument of the suggested SCDAMLI topology.

The inverter losses are mainly conduction and switching losses of the semiconductor devices. The conduction losses take place when the current passes through the switches and is calculated by the voltage drop across the devices in the on-state and the equivalent resistance of the devices [18]. Switching losses are incurred during turn-on and turn-off losses and they are dependent on the switching energy and the switching frequency. With the expressions above one can get the total inverter loss by adding these two components together. With the parameters of the simulation and the properties of the device applied in this study, the overall losses will be comparatively low because the number of switches will be reduced, and the switching strategy will be optimized.

2.2 Operating Modes of the Proposed SCDAMLI

The suggested Single-Carrier Driven Asymmetric Multilevel Inverter (SCDAMLI) has multiple different modes of operation based on the energy source used, load conditions as well as the charging or regenerating conditions [5]. The selective activation of unidirectional and bidirectional switches which control each operating mode, is what governs the conduction path of current through the inverter and the DC sources associated with the current.

Mode 1 (M1): Inverter is in its normal steady-state operation during which the primary DC source Va provides power to the load. Switches S2, S3 and S5 are left ON, and S1 can be closed as well to create the connection with Va. The current is taken through Va→S2→S3→S5→Load. This will be the normal working state of continuous power supply.

Mode 2 (M2): the second DC supply Vb, delivers power to the load which is a backup in case Va is off. Here, switches S7, S9, S10, and S5 will be ON and all the others will be OFF. The present route is Vb→S7→S9→S10→S5→Load.

Mode 3 (M3): is the high power or burst operation mode which uses the super capacitor-based DC source Vc to supply momentary power to the load. Switches S6, S8, S11 and S5 are turned ON and other switches are turned off. The current is flowing through Vc→S11/S8→mid-rail→S5→Load. The mode helps in stabilizing the voltage of the buses during sudden changes in loads or during peak periods.

Mode 4 (M4): the Va and Vb are parallel to distribute the load current. S2, S3, S5, S7 and S9 are switched ON (interconnection switches are closed when they are used). The current of Va plus Vb is sent through S5 to the load and it distributes stress between sources making systems more efficient.

Mode 5 (M5): is charging in which Vb is refilled by power of Va. Switches S1, S5, S7 and S12 are on, but S2, S3, S9 and S10 are off. The current path is Va→S1→S5→S7→S12→Vb. This regulated flow keeps Vb at its desired potential with no influence on the load.

Mode 6 (M6): of operation allows the charging of the Vc either due to Va or due to the regenerative power present on the DC bus. Switches S1 (or S5), S6 and S11 are turned on and S2 and S3 are kept off to isolate the load. The current of the bus or Va passes through S5, S6, and S11 to charge Vc, energy is well managed between the sources.

Mode 7 (M7): is the inverter which operates in the regenerative energy recovery mode. Any surplus power by the load is passed through to charge the storage devices Vb or Vc. In this case, switches S9, S11 (or S12), and S5 are turned on, and S2 and S3 are turned off to isolate Va. The load energy is directed by S5 and S9 to S11 or S12 and thus the auxiliary DC sources are recharged under the conditions of braking or reverse direction movement of the vehicle.

Mode 8 (M8): is isolation or protection mode applied when doing system maintenance or fault conditions. All load-path switches, such as S5, S3, and S10 are open and are completely out of the load path with the inverter. This improves the safety of operators and any undesirable current flow when the operator is inactive.

Mode 9 (M9): inverter does the balancing of voltage between the two auxiliary sources Vb and Vc. Bidirectional switches S11 and S12 are turned on, and switches S2 to S5 are turned off, and switches S6 or S7 (depending on the direction of transfer that is required) are turned on. The energy flow is Vb S11/S12→ Vc. This balancing activity brings a balance between the state-of-charge of both energy storage units and ensures constant inverter performance.

Mode 10 (M10): is the soft-start or pre-charge mode. In this configuration the precharge supply is first connected and switching S5 is gradually made and increasing connection to S1 and S2 is performed. All other power switches are kept off to control high inrush currents. The precharge current is directed to the precharge circuit to the DC bus and then to the load when voltage stability is attained.

The proposed SCDAMLI will need three isolated DC voltage sources to produce the 23 voltage levels.

The asymmetric magnitude of the voltage helps the topology to realize many levels and fewer sources as compared to the traditional cascaded multilevel inverter topology. In general, these mode of operations indicate the flexibility and smartness of the suggested SCDAMLI topology.

The inverter can effectively control the multi-source power delivery [3], and energy storage charging, regenerative recovery and system protection by coordinated switching actions, thus providing greater reliability as well as better dynamic performance across the changing operating conditions.

2.3 Control Strategy

Figure 5 shows the PV system structure, whereas Figure 6 shows the suggested control scheme of the SCDAMLI-based system. To achieve the control strategy, the dq0-synchronous reference frame technique is adopted where the three-phase source voltages are converted to the dq0-frame through the transformation given by Park as shown below.

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \sin(\omega t) & \sin(\omega t - 120) & \sin(\omega t + 120) \\ \cos(\omega t) & \cos(\omega t - 120) & \cos(\omega t + 120) \\ 1/2 & 1/2 & 1/2 \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (22)$$

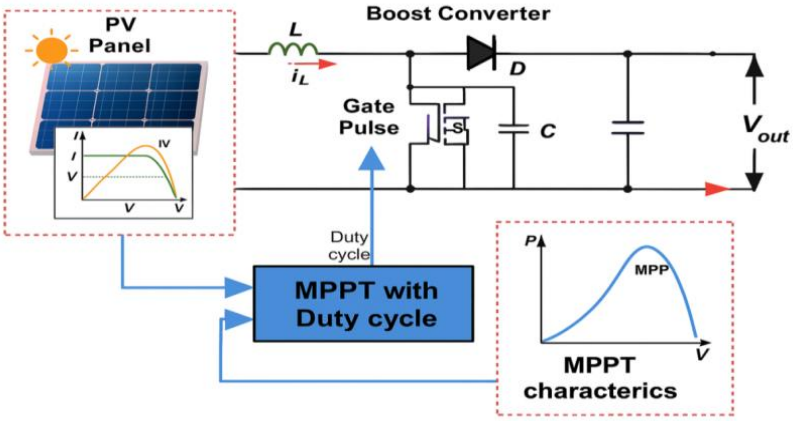


Figure 5. Photovoltaic (PV) Array setup of the Proposed SCDAMLI System

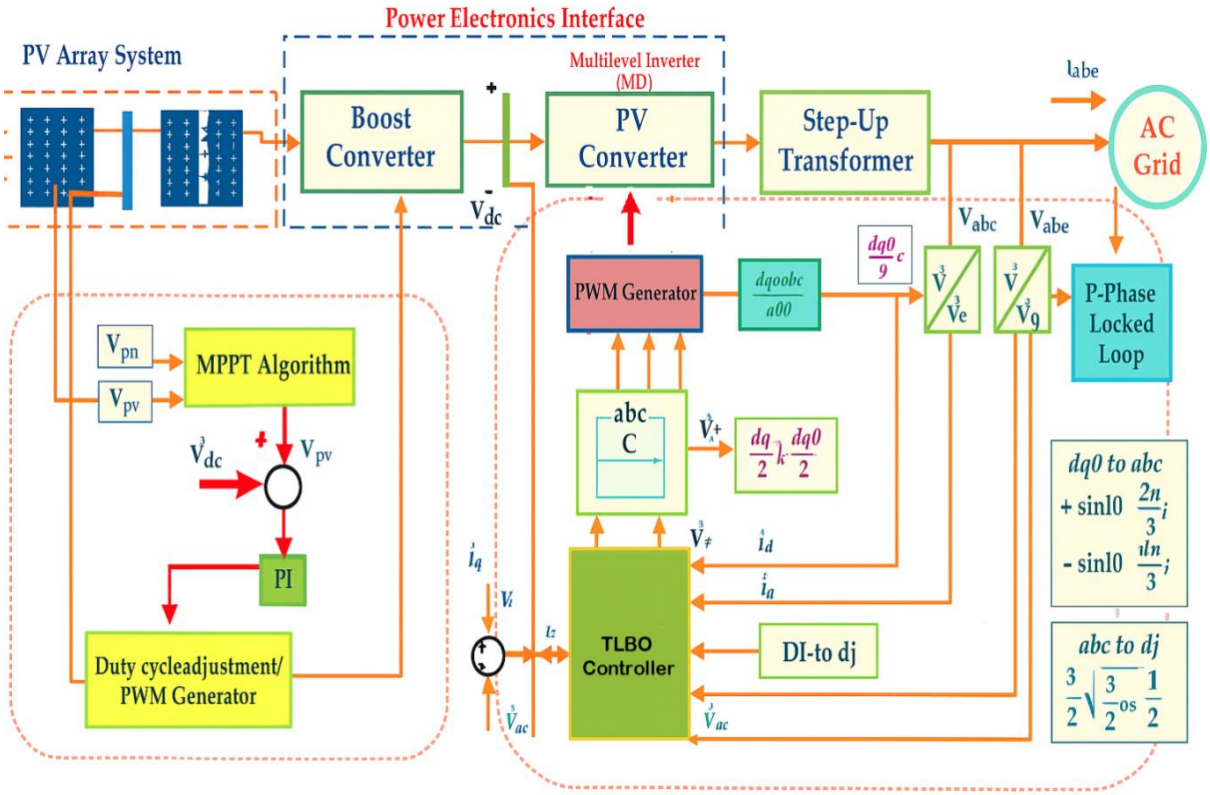


Figure 6. Control Scheme of the Suggested SCDAMLI-Based System

The resultant dq0 values are compared to the reference values (d=1, q=0) and the error signal is handled by an ANFIS (Adaptive Neuro- Fuzzy Inference System) controller [19]. The TLBO (Teaching-Learning-Based Optimization) algorithm also tunes the error to produce optimized dq0 components [20]. These tuned dq0 signals are once again transformed to the ABC frame with the inverse Park transformation as below equation.

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \sin(\omega t) & \cos(\omega t) & 1 \\ \sin(\omega t - 120) & \cos(\omega t - 120) & 1 \\ \sin(\omega t + 120 & \cos(\omega t + 120) & 1 \end{bmatrix}\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} \quad (23)$$

The ANFIS structure is a first-order Sugeno-type system with two inputs and one output. The inputs are the PV error E(k)=dPdVE(k)=\frac{dP}{dV}E(k)=dVdP and change in error ΔE(k)\Delta E(k)ΔE(k), and the output is the reference duty cycle DrefD_{ref}Dref for the boost converter. Each input uses five triangular membership functions (NB, NS, ZE, PS, PB), resulting in 25 fuzzy rules. Hybrid learning (least-squares + backpropagation) is employed for parameter tuning.

The training dataset was generated using simulated PV characteristics under irradiance levels ranging from 200–1000 W/m² and temperatures from 25–50°C. 70% of the dataset was used for training and 30% for validation to avoid overfitting [21].

MPPT performance was evaluated under standard irradiance transients (1000→600→800 W/m²) and temperature variation (25°C→45°C). The controller achieved:

- Tracking efficiency > 99.1%•
- Settling time < 0.03 s
- Steady-state oscillation < 0.5%
- Negligible overshoot in duty response

These additions clarify the ANFIS structure, reproducibility, and dynamic performance under realistic operating conditions.

The resulting signals (ABC frame) are used to produce gate pulses to the IGBT-based three-leg VSI by means of pulse-width modulation (PWM) method [22]. At the inverter output, an LC filter is added to reduce the harmonics and provide a smooth voltage of AC waveform to the load [23]. A voltage injection transformer is used to inject a compensating voltage in order to stabilize the grid in the presence of load voltage disturbances.

This control system enables the harmonic mitigation and better quality of voltage at the load, through adjusting the dq0 error signals [24]. Both TLBO-optimized controller and a traditional PI controller are used to analyze the system performance, and the two are compared with each other.

2.4 TLBO Optimization Algorithm

The Teaching-Learning-Based Optimization (TLBO) algorithm is used to optimize switching angles of the proposed MLI as shown in Figure 7. Parameters of optimization: the number of iterations is set to 5000; the modulation index (MI) = 0.01:0.01:1; $\alpha = \mathrm{X}; \mathrm{Xmax} = \left[\frac{\pi}{2}\ \frac{\pi}{2}\ \frac{\pi}{2}\ \frac{\pi}{2}\ \frac{\pi}{2}\right]$ (in degrees) and Xmin=[0,0,0,0,0]; population size N=10×n, where n is the length of Xmax; and teaching factors r=0 or 1, T_f=1 or 2.

The TLBO optimization problem is developed to reduce the cost formulation:

$$f(\alpha_1, \alpha_2, \alpha_3, \alpha_4, \alpha_5) = \min\left[\left|100 * \left|\frac{|V_{\text{desired}} - V_1|}{V_{\text{desired}}}\right|^4 + \sum_{s=2}^{s} \frac{1}{h_s}\left|50\frac{V_{h_s}}{V_1}\right|^2\right|\right] \quad (24)$$

whereV1 = the basic part of inverter output Vrms = the voltage on the terminal, and hs is the harmonic order. The percentage voltage Total Harmonic Distortion (% V-THD) is determined as:

$$\%\mathrm{V} - \mathrm{THD} = \left(\sqrt{\left(\frac{V_{rms}}{V_1}\right)^2 - 1} *\right) * 100 \quad (25)$$

With this formulation, the TLBO algorithm can choose optimal switching angles to achieve minimum harmonic distortion but still deliver the desired fundamental output voltage, which gives the algorithm a foundation to compare its performance with traditional PI-based controllers.

The TLBO reproducibility details have now been clearly specified. The decision variables are the five switching angles α1, α2, α3, α4, α5 for the 23-level inverter. The constraints are 0<α1<α2<α3<α4<α5<π to ensure proper harmonic elimination and waveform symmetry. The cost function minimizes fundamental voltage deviation and selected lower-order harmonics using a weighted THD-based objective formulation. The final optimized switching angles corresponding to the modulation index range (MI = 0.8–1.0) have been tabulated in the revised manuscript to reproduce the reported THD results.

2.5 Simulation Setup

The proposed system was implemented in MATLAB/SIMULINK environment to validate the performance of the SCDAMLI topology. The simulation parameters used in the study are summarized in Table 3.

3. Results and Discussion

3.1 Results

MATLAB/SIMULINK was used to test the performance of the proposed 23-level SCDAMLI.

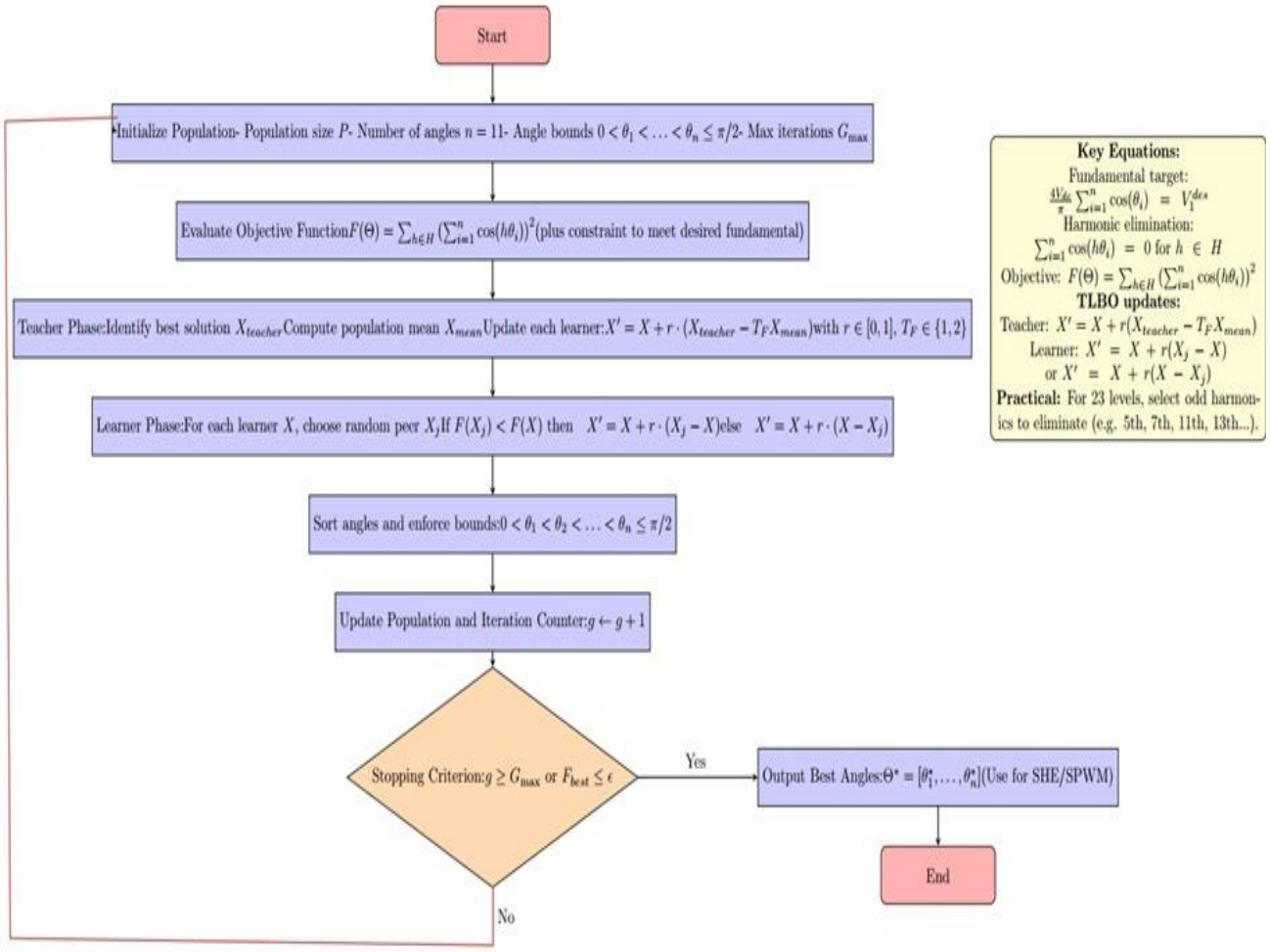


Figure 7. The flowchart of the Teaching-Learning-Based Optimization (TLBO) Algorithm

Table 3. Parameters used in proposed system

Category	Parameter	Value
Grid Conditions	Grid Voltage (Line–Line RMS)	415 V
	Grid Frequency	50 Hz
	Grid Impedance (Rg, Lg)	0.1 Ω, 2 mH
DC Sources	(V_a)	50 V
	(V_b)	150 V
	(V_c)	350 V
Load Parameters	Load Type	RL Load
	Load Resistance (R)	422.5 Ω
	Load Inductance (L)	5 mH
Filter Parameters	Output Inductor (Lf)	3 mH
	Output Capacitor (Cf)	20 µF
PWM Arrangement	Modulation Technique	SPWM with Phase Disposition (PD)
	Carrier Frequency ((f_s))	3 kHz
	Fundamental Frequency ((f_m))	50 Hz
	Modulation Index (MI)	0.8 – 1.0
Control Parameters	TLBO Iterations	5000
	Population Size	10 × number of angles
Simulation Setup	Sampling Time	5 µs
	Solver Type	ode23tb (stiff/TR-BDF2)
	Simulation Step Size	1e-6 s

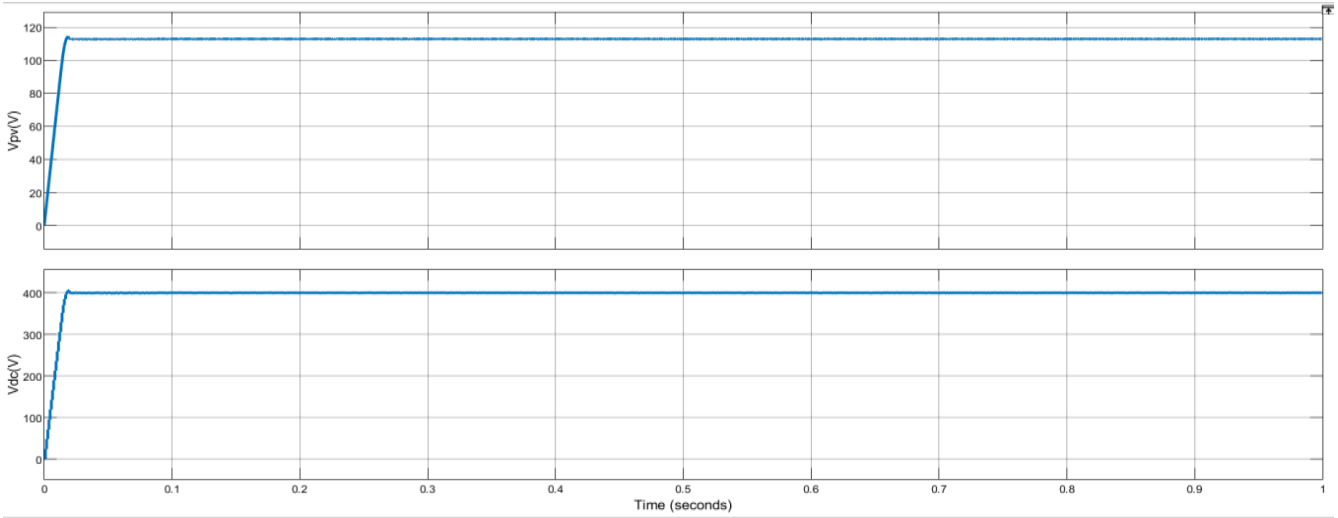


Figure 8. DC link voltage and solar PV output voltages to the SCDAMLI

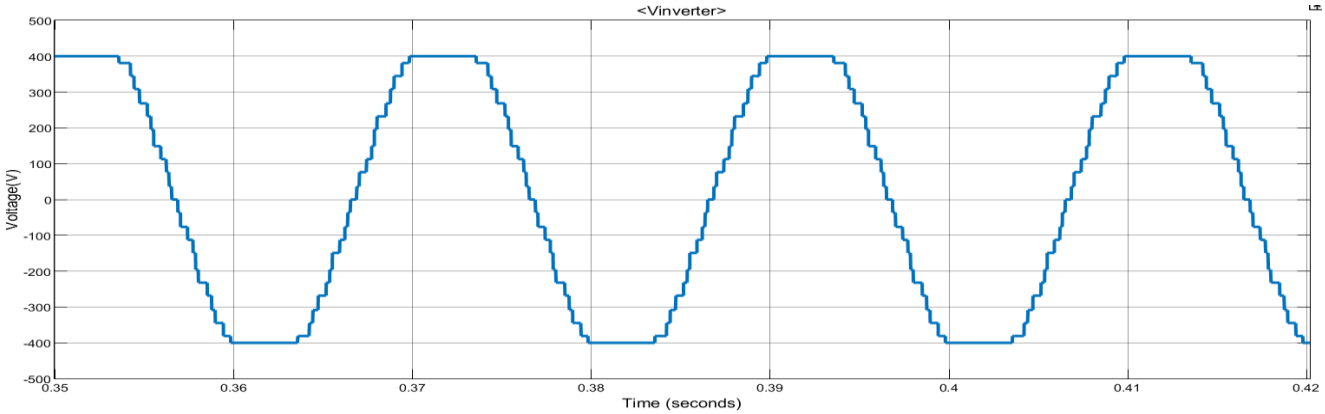


Figure 9. SCDAMLI output voltage waveform of 23-levels

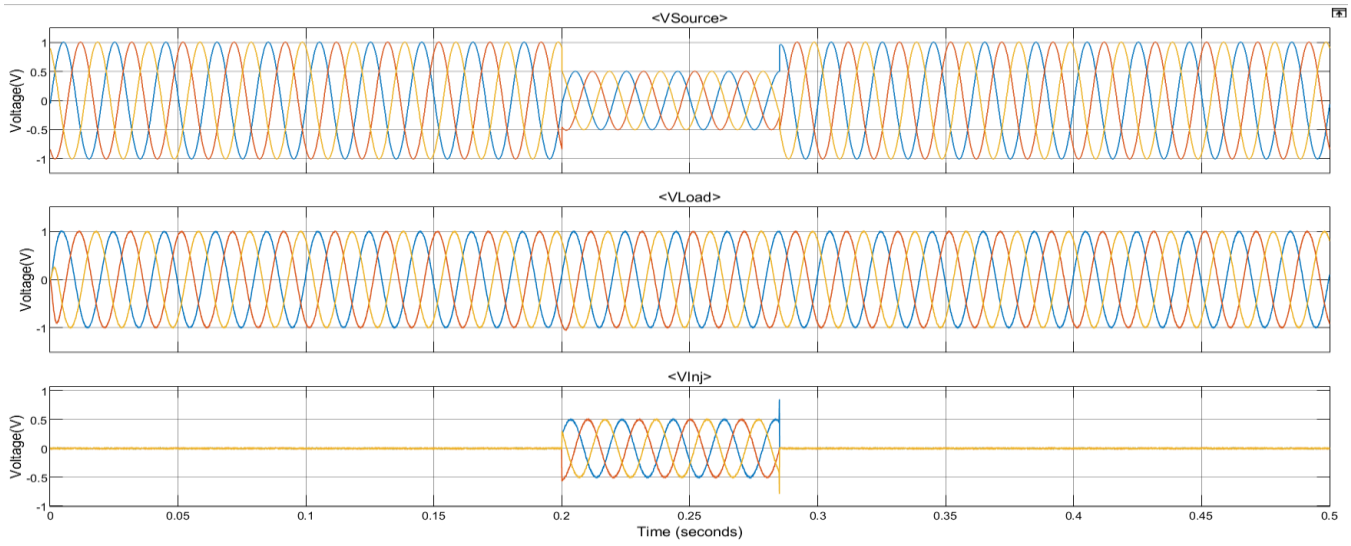


Figure 10. Compensation of Voltage sag 30% with SCDAMLI as a series controller

The system is designed with the TLBO-based control scheme in order to optimize switching angles and enhance harmonic performance. Figure 8 indicates the DC link voltage and the solar PV output voltages in the input of the inverter. The inverter produced a 23-level output voltage waveform as shown in figure 9. The waveform shows distinct multilevel steps with enhanced sinuosity.

The inverter suggested has twelve switching devices that include five bidirectional switching branches together with seven unidirectional switches.

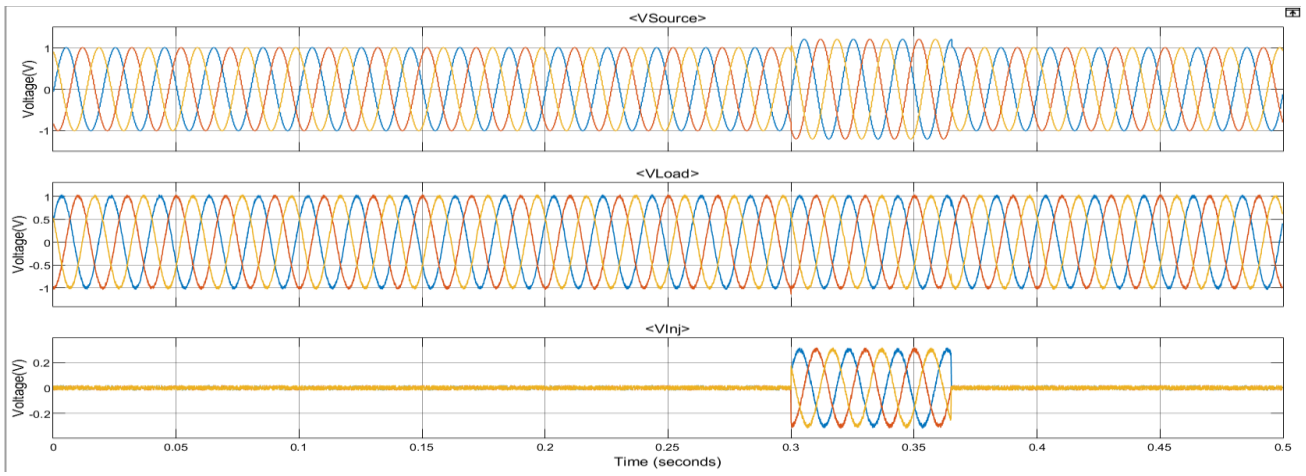
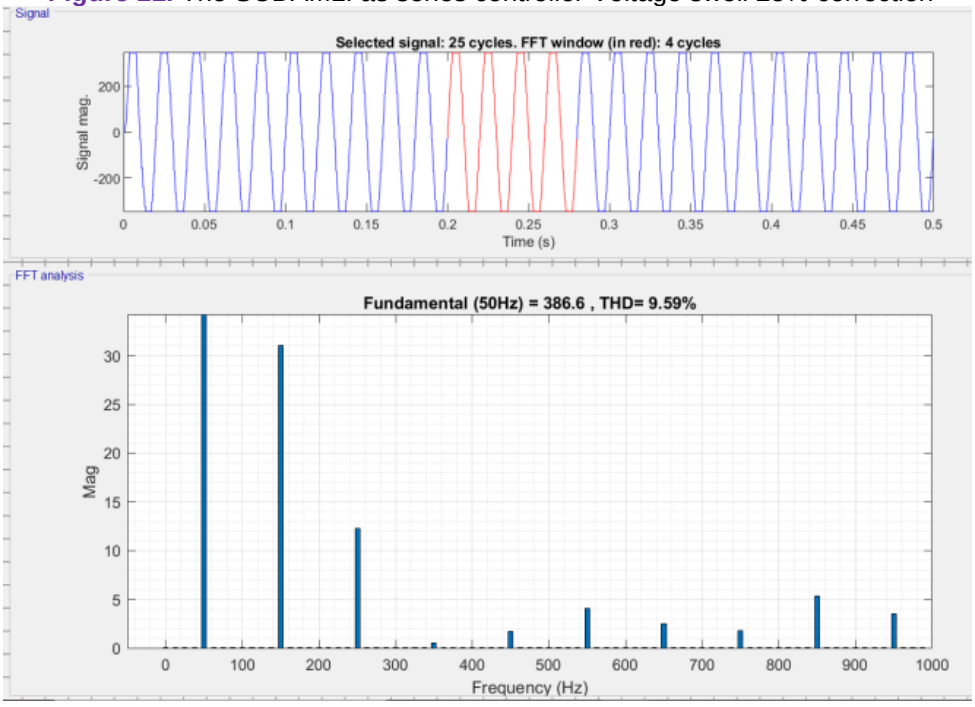


Figure 11. The SCDAMLI as series controller Voltage swell 25% correction

(a)



(b)

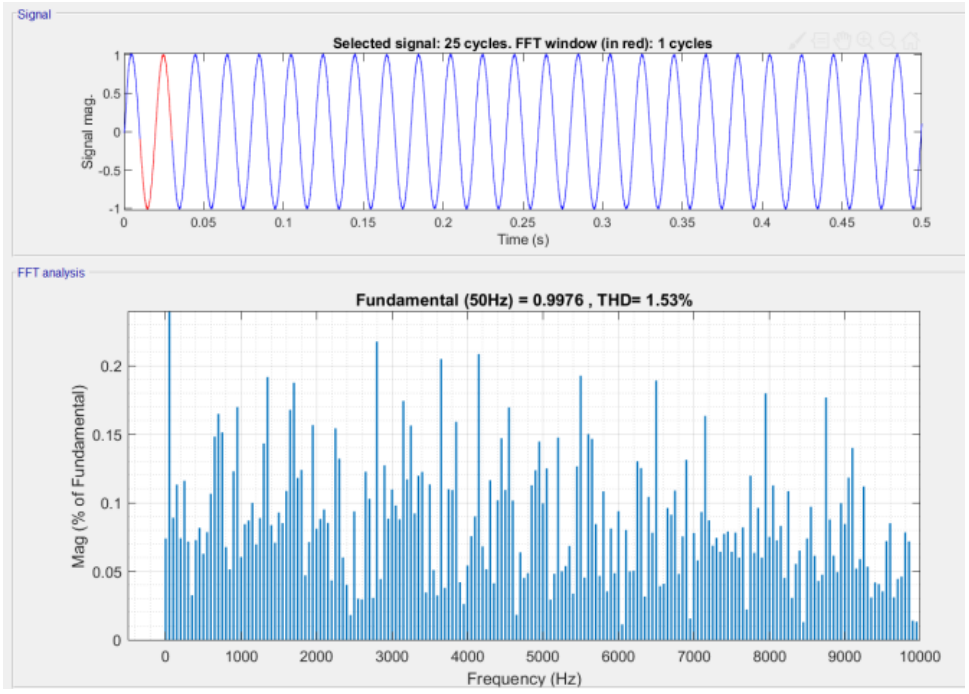


Figure 12. FFT of the result with TLBO-based control of the percentage of THD

The inverter will then need twelve channels of gate-driving since one switching device must have its individual gate control signal. The lower switching number than in the traditional multilevel inverter circuitry thus reduces the gate-driver circuitry and implementation complexity.

The ability of the SCDAMLI to compensate voltage sag and swell in case of the solution as a series controller is demonstrated in figures 10 and 11. Between 0.2s-0.3s, voltage sag was injected and between 0.3s-0.4s swell was injected. The proposed system effectively cancels both sag and swell, and the voltage at the load side is almost a pure sinusoid.

The win parameters are so: primary switching frequency fm=50 Hz, carrier frequency fs=3000 Hz, load RL=422.5 Ω, DC sources V_{dc1}=50V, V_{dc2}=150V, V_{dc3}=350V. Figure 9 presents the inverter output voltage waveform of the proposed SCDAMLI. The inverter output passes through an LC filter to cause the harmonic distortion to be minimized and the output is a near-sinusoidal voltage waveform [1]. The FFT spectrum of the inverter output is shown in Figure 12. The overall voltage THD of the proposed SCDAMLI is less than 1.53 percent with each of the harmonic less than 5 percent, which indicates a high level of harmonic reduction [13, 16, 15].

3.2 Discussion

To compare the benefits of the proposed asymmetric SCDAMLI topology with traditional multilevel inverter (MLI) topologies, such as Neutral Point Clamped (NPC-MLI), Flying Capacitor (FC-MLI) and Cascaded H-Bridge (CHB-MLI) topologies are compared. To have the same level of output voltage, Table 4 summarizes the number of switches and DC sources that are required with each topology. An output voltage of 23 levels is regarded as a reference in computing components in any topology.

Table 4. Switch and DC Source Requirement Comparison between SCDAMLI and Traditional MLIs

Topology	Number of Switches	Number of DC Sources	Reference
NPC	6(N-1)	(N-1)	[1], [2]
FC	6(N-1)	(N-1)	[1], [2]
CHB	6(N-1)	3(N-1)/2	[3]
Proposed	$n_s^{Asy} = \frac{(n_l+1)}{2}$	$n_{dc}^{Asy} = \frac{(n_l-5)}{6}$	-

Even though the proposed topology will have 12 switches. Every bidirectional switch is implemented by connecting two unidirectional switches in emitter format, each bidirectional switch only needs one driver circuit. Table 3 indicates that the proposed asymmetric MLI generates the same output voltage using a smaller number of components which means reduced cost and also higher efficiency.

Table 5 is the comparison of the proposed system with the existing 23-level MLI topologies in the respect of voltage THD, DC sources, and switch. The findings underline the fact that the proposed SCDAMLI has reduced THD but fewer components.

Table 5. Percent THD, Switch and DC Sources Count of 23 Level MLIs

Reference	N_{lev}	N_{DC}	N_{SW}	%THD
[16]	23	5	12	4.17
[19]	23	5	12	3.6
[5]	23	3	12	--
[15]	23	6	12	2.59
[20]	23	5	10	--
[23]	23	5	14	5.47
Proposed	23	3	12	1.53

The efficiency of the proposed inverter is determined by assessing the amount of power that was put across into the load and the summation of the input power in the DC sources. The efficiency is computed on various load conditions to confirm the operation of the topology. The received results prove that the inverter could be of high efficiency under a large operating range because of fewer switching losses and optimal voltage synthesis. The comparison shown in Table 5 suggests that the proposed SCDAMLI has lower THD (1.53%), in comparison to topologies that are currently available with 23 levels with fewer DC sources needed.

4. Conclusion

The paper presents a new Smart Control-Driven Asymmetric Multilevel Inverter (SCDAMLI) with the ability to generate 23-levels output voltage with the lowest number of power semiconductor switches. This topology is proposed and it is efficient in making use of several switching states to attain the intended voltage levels with less active switches. The inverter is also adaptable by construction to be integrated with renewable energy sources, such as solar, wind, and biomass, by the use of asymmetrical DC sources. The proposed inverter was further tested to confirm its performance in relation to a FACTS device that is based on DVR at different operating conditions. The proposed SCDAMLI produces 23 levels of output voltage with three DC sources and twelve switches which is much less complex than the usual multilevel inverter topologies. A THD of 1.53% at LC output filter is shown by simulation, within IEEE 519 harmonic limits. The lower number of components, higher harmonic functionality and more efficient TLBO control plan make

the proposed topology a good choice in renewable energy and grid inter-connection. Comparison with traditional MLI topologies showed that there were high reductions in the number of components, the size of the system and the cost of implementation. On the whole, the proposed SCDAMLI illustrates an encouraging and effective solution to renewable energy integration, which has better quality of voltages and less complexity of the components, as well as, higher cost-effectiveness.

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Authors Contribution Statement

C. Dinakaran: Conceptualization, Methodology, Software Implementation, Writing Original Draft. T. Padmavathi: Investigation, Formal Analysis, Visualization, Supervision. Both Authors Read and Approved Final version of the manuscript.

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The authors declare that there are no conflicts of interest regarding the publication of this manuscript.

Data Availability

The data supporting the findings of this study can be obtained from the corresponding author upon reasonable request.

Has this article screened for similarity?

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